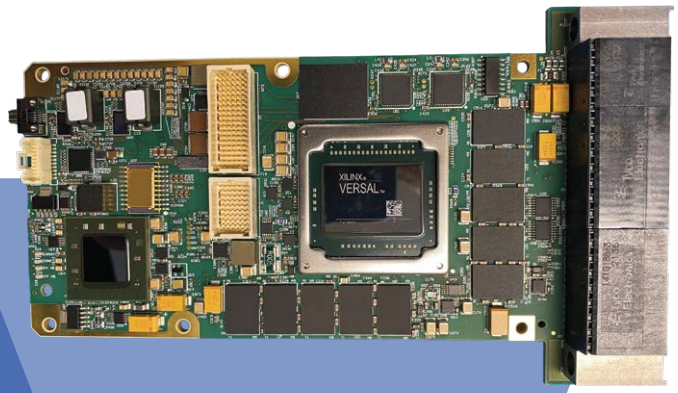
VDRT

VERSAL DIGITAL RF TRANSCEIVER

The VDRT is a revolutionary 3U VPX processor based on the Xilinx VC1902 Adaptive Compute Acceleration Platform (ACAP) with AI core. The VDRT will provide never-before available processing power and mezzanine expansion in an industry leading C-SWaP product.



Breakthrough Performance in a 3U VPX Module

RF and Processing On The Edge

Trident's VDRT leverages the full capability of the revolutionary Xilinx Versal ACAP. The VDRT combines Scalar Engines, Adaptable Engines, Intelligent Engines in a fully software programmable platform. Built on Trident's demonstrated 3U VPX architecture, the VDRT will enable a wide range of on-oribt RF and processing previously not available.

Mission Enabling

A proven Radiation Effects Mitigated architecture, coupled with radiation tolerant components, redundancy and a robust mechanical design, provide a low C-SWaP, high reliability module for a wide range of applications. Hardware, Software, Firmware customization available with a wide range of FW/SW deployment options.

TRIDENT
SPACE ELECTRONIC SYSTEMS
A LIGHTRIDGE SOLUTIONS COMPANY

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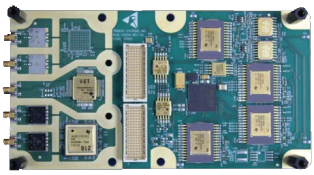
Versal Digital RF Transceiver

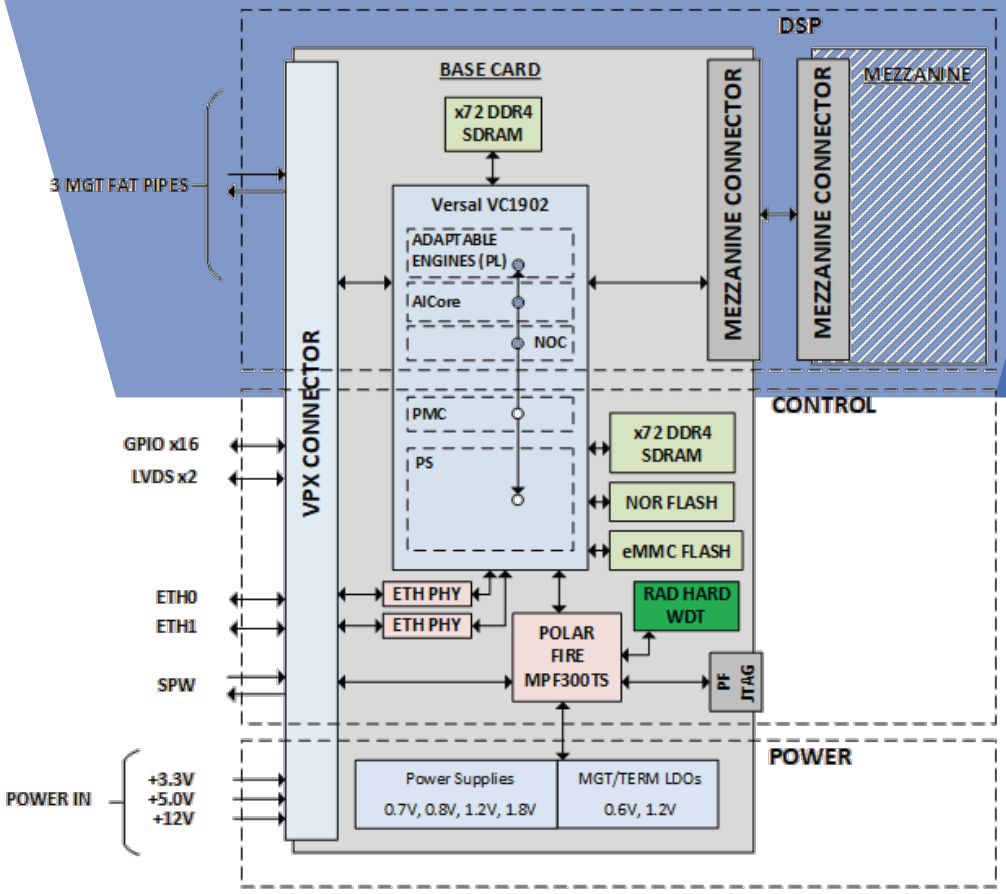
Mezzanine Options

ADC/DAC/PLL



SSD Storage

Custom - Contact Us



Specifications

SWaP	3U VPX, 1" pitch, < 900g, ~TBD W (TYP), +65 C rail temp
Processor	Xilinx Versal AI Core XCVC1902-1MSIVIVA1596 Programmable Network on Chip (NoC)
Memory	Two (independent) 8 GB [TBR] x72 DDR4 Memory Banks with ECC DDR4 banks are assignable based on application 32 GB (minimum) NAND Flash; 256 MB Redundant NOR Flash
I/O	PCIe Gen4 compliance; 32.75 Gb/s transceivers
Mezzanine Site	14GTYs transceivers Compatible with ADC/DAC/PLL, SSD, and Custom Mezzanine Cards
Fault Tolerance	Configuration Upset Immune PolarFire System Controller RHBD Watchdog Timer
Reliability	Versal: no SEL and meets 5-7 year TID for LEO missions Balanced design assurance plan for Class B-D Missions

VC1902 Features

Ruggedization	7nm radiation tolerant SoC
Application Processing Unit	Dual-Core ARM CortexTM-A72
Real-Time Processing Unit	Dual-core ARM CortexTM-R5F
AI Core Engines	400
Programmable Logic (PL)	899,840 LUTs, 191Mb Block RAM, 1,968 DSP Slices

VDRT DEVELOPMENT KITS AVAILABLE

Contact Us: SES-BD@tridsys.com